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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/091,743	03/06/2002	Danielle A. Thomas	01-C-086 (STMI01-01086)	8460	
7590 06/30/2005			EXAMINER '		
Lisa K. Jorgenson, Esq. STMicroelectronics, Inc. 1310 Electronics Drive Carrollton, TX 75006			NGUYEN, DONGHAI D		
			ART UNIT	PAPER NUMBER	
			3729		
			DATE MAILED: 06/30/2009	DATE MAILED: 06/30/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)				
Office Action Commons	10/091,743	THOMAS ET AL.				
Office Action Summary	Examiner	Art Unit				
	Donghai D. Nguyen	3729				
~ The MAILING DATE of this communication appears on the cover sheet with the correspondence address — Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed on <u>06 May 2005</u> .						
2a) This action is FINAL . 2b) ⊠ This	This action is FINAL . 2b)⊠ This action is non-final.					
3) Since this application is in condition for allowar	3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4)⊠ Claim(s) <u>1-22</u> is/are pending in the application.						
4a) Of the above claim(s) <u>11-22</u> is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1,2 and 10</u> is/are rejected.	6)⊠ Claim(s) <u>1,2 and 10</u> is/are rejected.					
7)⊠ Claim(s) <u>3-9</u> is/are objected to.	7) Claim(s) 3-9 is/are objected to.					
8) Claim(s) are subject to restriction and/or	election requirement.					
Application Papers						
9)☐ The specification is objected to by the Examiner.						
10)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of:						
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).						
* See the attached detailed Office action for a list of the certified copies not received.						
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Attacheroute						
Attachment(s) 1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)						
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date						
i) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5) Notice of Informal Patent Application (PTO-152) 6) Other:						
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DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of invention Group I, claims 1-10, in the reply filed on May 06, 2005 is acknowledged. The traversal is on the ground(s) that the integrated circuit recited in claim 11 cannot made by another and materially different process and The Patent Office cannot ignore express recitations in the claims when making restriction. This is not found persuasive because the Patent Office can ignore the recitations in the product by process claimed. See MPEP § 2113 and *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). Therefore, claim 11 does not require etching because it is a product claim.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 103

- 2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 3. Claims 1, 2, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,441,467 to Toyosawa et al in view of US Patent 6,180,445 to Tsai.

Regarding claim 1, Toyosawa et al disclose a method for fabricating an integrated circuit comprising the steps of: fabricating a portion of the integrated circuit (semiconductor device, see Fig. 1), the portion comprising at least one active circuit area (active element 20); fabricating a redistribution metal layer (14) over the at least one active circuit areas; However, Toyosawa et el

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deposit a silicone nitride layer over at least a portion of the redistribution metal layer and etching the silicone nitride layer to leave at least one portion of the redistribution metal laver open to receive at least one solder bump in stead of polyimide layer as cited in claims 1, 4 and 9. Tsai teaches that a polyimide layer has many advantages such as providing partial planar surface and deposit and etching polyimide layer is simple (See, Col. 4, line 64 to Col. 5.ine 16). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Toyosawa et al by substituted the silicone nitrate layer with the polyimide layer as taught by Tsai for polyimide layer providing partial planar surface and the step of depositing and etching polyimide layer is simple.

Regarding claim 2, Fig. 1 of Toyosawa et al shows at least one flat portion of the redistribution metal layer to receive the at least solder bump (30).

Regarding claim 10, Figs. 4f and 13b of Toyosawa et al show the redistribution metal layer using a last metal layer that is used to fabricate the active circuit area of the integrated circuit.

Allowable Subject Matter

- 4. Claims 3-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 5. The following is a statement of reasons for the indication of allowable subject matter: the prior art references do not teach or suggest a specific method step of: "depositing the redistribution layer over the silicon oxynitride layer and in electrical connection with the vertical

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plug" as recited in claim 3 and a step of: "depositing a silicon oxynitride layer over at least some portion of redistribution layer" in combination with other limitations as recited in the claim 5. The best prior art, US Patent 6,441,467 discloses the method for making an integrated circuit but fail to teach or suggest the method steps as described in details above.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art references cited for the teaching of fabrication an integrated circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghai D. Nguyen whose telephone number is (571)-272-4566. The examiner can normally be reached on Monday-Friday (9:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter D. Vo can be reached on (571)-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DN

June 20, 2005